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A Comparative Analysis of Improved 8T SRAM Cell With Different SRAM Cell

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Abstract
High speed and low power consumption have been the primary issue to design Static Random Access Memory (SRAM), but we are facing new challenges with the scaling of technology. The stability and speed of SRAM are important issues to improve efficiency and performance of the system. Stability of the SRAM depends on the static noise margin (SNM) so the noise margin is also important parameter for the design of memory because the higher noise margin confirms the high speed of the SRAM cell. In this paper, The proposed improved 8T SRAM cell shows maximum reduction in power consumption of 24.17% with 6T, of 88.6% with 7T, of 28.21% with 8T and of 35.03% with 9T, maximum reduction in delay of 9.1% with 6T, of 64.26% with 7T, of 9.18% with 8T and of 10.44% with 9T and maximum SNM of 35.02% with 6T, of 32.27% with 7T, of 34.4% with 8T and of 33.15% with 9T increases.
Keywords- Cadence tool, CMOS logic, Static Noise Margin, Delay and Power Consumption.

I. INTRODUCTION

Static Random Access Memory is a type of RAM used in various electronic applications including toys, computers, digital devices and automobiles. The static RAM or SRAM only holds its contents while power is applied. An SRAM cell keeps the cell data for as long as the power is turned on since it consists of a latch and refresh operation is not required for the SRAM cell. Its difference from dynamic RAM is that DRAM must use refresh cycles to keep its contents alive. As indicated by the name, SRAM holds data/memory as a static image until written over or lost from powering down. SRAM is mainly used for the cache memory in microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to high speed and low power consumption. Each bit in an SRAM is stored on four transistors that form two cross coupled inverters. Static Random Access Memories (SRAMs) are commonly embedded into system-on-chip (SoC) designs to store programs and data. Many efforts have been made to improve the efficiency of the SRAM. Improvements are reducing delay, power consumption and increasing stability. A significant increase has been there in the demand for low power and high performance digital VLSI circuits. Designers are implementing very high-order scaling of both device dimensions and supply voltage. Transistor density and functionality on a chip is improved by scaling. Scaling also helps to increase speed and frequency of the operation and hence higher performance. This paper is presented an improved 6T SRAM cell that has low power consumption & high static noise margin than the other different SRAM cell.

II. THE LITERATURE REVIEW OF DIFFERENT SRAM CELLS

2.1 6T SRAM CELL

A. Construction

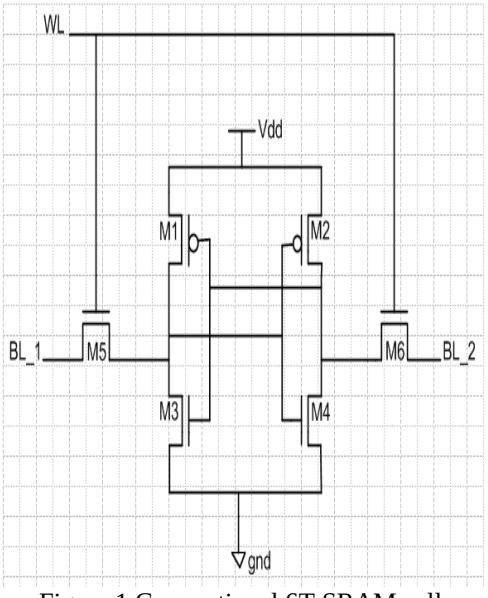

Figure 1 Conventional 6T SRAM cell

The SRAM cell is the key component for storing the binary information. By the use of two cross-coupled inverters, a typical SRAM cell forms a latch and access transistors. The access transistors enable access to the cell during read and write operations and provide cell isolation during the not-accessed

state. SRAM cell is designed to provide write capability, non-destructive read access and data storage (or data retention) for as long as cell is powered. The design and analysis of different SRAM cells are: Conventional 6T, 7T, 8T, 9T and improved 6T. They are compared with respect to power, delay and speed. Generally, the cell design must strike a balance between cell area, speed, robustness, leakage and yield. One of the most important design objectives is power reduction. However, power cannot be reduced indefinitely without compromising the other parameters. As an example, low-power can compromise the cell area and also the speed of operations. The mainstream six-transistor (6T) CMOS SRAM cell is shown in Figure -1, here four transistors (M1−M4) comprise cross-coupled CMOS inverters and two NMOS transistors M5 and M6 provide read and write access to the cell. The most popular SRAM cell is a 6T CMOS SRAM cell due to its superior robustness, low-voltage and low power operation [9].

B. Operation of SRAM

The Static Random Access memory device can perform the operation which is as follows: hold, read and write.

a. Hold: The access transistors M5 and M6 disconnect the cell from the bit lines, if the word line is not asserted. The two cross coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

b. Read:

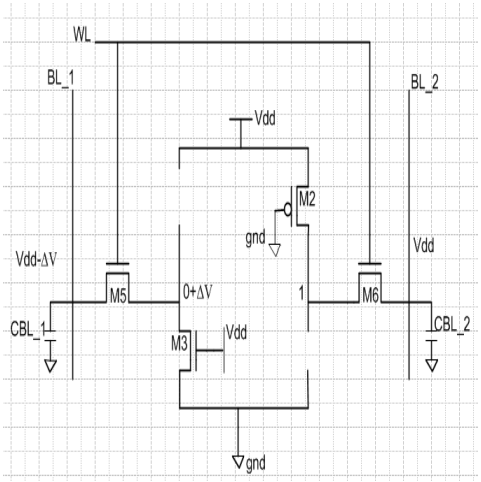

Figure 2 Read Operation of SRAM Cell.

The bit lines are pre-charged to VDD prior to initiating a read operation. The read operation is initiated by enabling the word line (WL) and connecting the pre-charged bit lines (BL_1 and BL_2) to the internal nodes of the cell. On read access, the bit line voltage VBL_1 remains at the pre-charge level as shown in Figure-2. The complementary bit line voltage VBL_2 is discharged through transistors M1 and M5 connected in series. Conclusively, transistors M1 and M5 form a voltage divider whose output is now no longer at zero volts and is connected to the input of inverter M2−M4 (as in Figure -1). The sizing of M1 and M5 should ensure that inverter M2−M4 do not switch causing a destructive read [9].

c. Write:

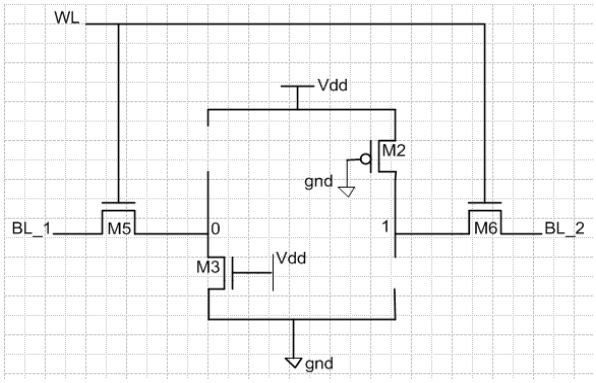

Figure 3 Write Operation of SRAM Cell.

While the write operation one of the bit lines i.e. BL_1 in Figure-3, is driven from pre-charged value (VDD) to the ground potential by a write driver through transistor M6. The cell is flipped and its data is effectively overwritten if transistors M4 and M6 are properly sized. A statistical measure of SRAM cell write ability is defined as write margin. The write margin is defined as the minimum bit line voltage required flipping the state of an SRAM cell. Write margin value and variation is a function of the process variation, SRAM array size and cell design. A cell is considered not writeable if the worst-case write margin becomes lower than the ground potential. The write operation is applied to the node storing a '1'. It is necessitated by the non-destructive read constraint that ensures that a '0' node does not exceed the switching threshold of inverter M2−M4. The only function of pull-up transistors is to maintain the high level on the '1' storage node and prevent its discharge by the off state leakage current of the driver transistor during data retention and to provide the low-to-high transition during overwriting [13]

2.2 7T SRAM CELL

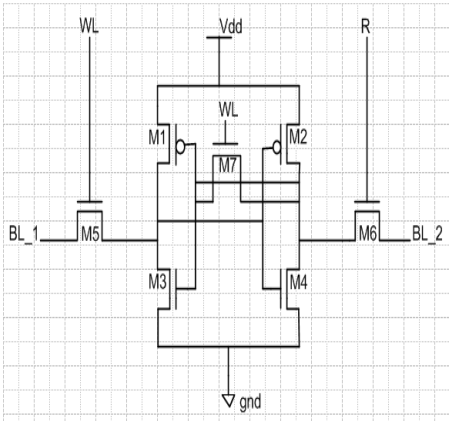

Figure 4 A 7T SRAM cell

The circuit of 7T SRAM cell is made of two CMOS inverters that are connected cross coupled to each other with additional NMOS Transistor which is connected to read line and has two pass NMOS transistors connected to bit lines and bit line bar respectively. Figure-4 shows circuit of 7T SRAM cell, where the access transistors M5 is connected to the word-line (WL) to perform the access write and M6 is connected to the Read-line (R) to perform the read operations thought the column bit-lines (BL_1 and BL_2). The bit-lines act as I/O nodes carrying the data from SRAM cells to a sense amplifier during read operation or from write in the memory cells during write operations [12].

2.3 8T SRAM CELL

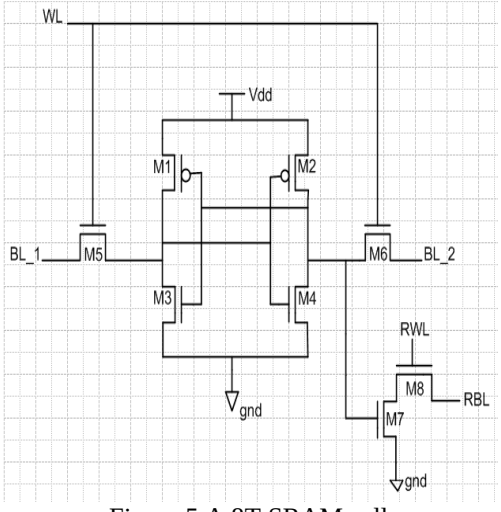

Figure 5 A 8T SRAM cell

The 8T SRAM circuit [13] is presented in this section. The schematic of the 8T SRAM cell sized for an 180nm CMOS technology is shown in Figure 5. The left sub-circuit of the 8T memory cell is a conventional 6T SRAM cell with minimum sized devices (composed of M1, M2, M3, M4, M5, and M6). Two data access transistors (M5 and M6) and two bit lines (BL_1 and BL_2) are used for writing to the SRAM cell. An alternative communication channel (composed of a separate read bit line RBL and the transistor stack formed byM7 and M8) is used for reading the data from the cell.

Two separate control signals RWL and WL are used for controlling the read and the write operations, respectively, with the 8T SRAM circuit as shown in Figure 5. During a read operation, the read signal RWL transitions to VDD while the write signal WL is maintained at VGND. The read bit line (RBL) is conditionally discharged based on the data stored in the SRAM cell. The storage nodes (Node1 and Node2) are completely isolated from the bit lines during a read operation. The data stability is thereby significantly enhanced as compared to the conventional 6T SRAM cells [13].

2.4 9T SRAM CELL

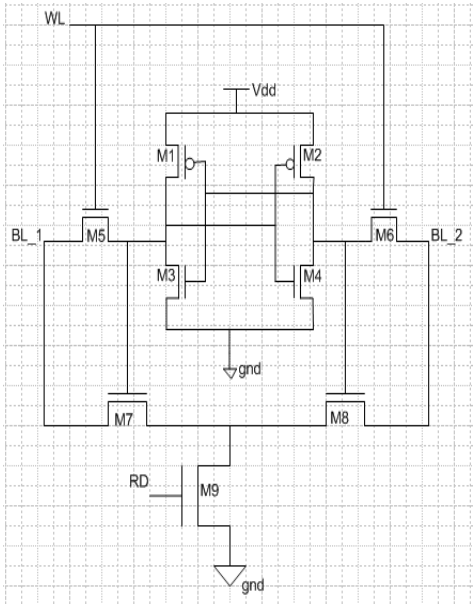

Figure 6 A 9T SRAM cell

A 9T SRAM cell is presented in figure-6. The upper sub-circuit of the new memory cell is essentially a 6T SRAM cell with minimum sized devices (composed of M1, M2, M3, M4, M5, and M6). The two write access transistors (M5 and M6) are controlled by a write signal (WL). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (M7 and M8) and the read access transistor (M9). The operations of M7 and M8 are controlled by the data stored in the cell. M9 is controlled by a separate read signal (RD). During a write operation, WL signal transitions high while RD is maintained low, as shown in Fig. 2(a). M9 is cut-off. The two write access transistors M5 and M6 are turned on. In order to write a "0" to Node1, BL_1 and BL_2 are discharged and charged, respectively. A "0" is forced into the SRAM cell through M5.

Alternatively, for writing a "0" to Node2, BL_1 and BL_2 are charged and discharged, respectively. A "0" is forced onto Node2 through M6. During a read operation, RD signal transitions high while WL is maintained low and the read access transistor M9 is activated. Provided that Node1 stores "1". BL is discharged through M7 and M8. Alternatively, provided that Node2 stores "1", the complementary bit line (BL_2) is discharged through M8 and M9. Since M5 and M6 are cut-off, the storage nodes Node1 and Node2 are completely isolated from the bit lines during a read operation [14].

III. IMPROVED 8T SRAM CELL

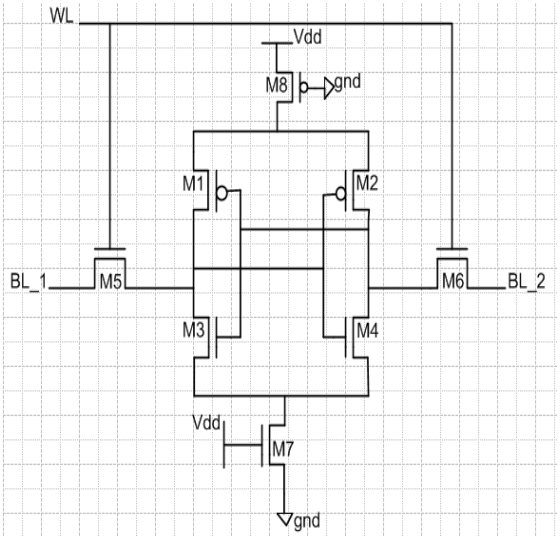

Figure 7 Improved 8T SRAM cell

The proposed SRAM cell is shown in Figure 7; it is made of conventional 6T SRAM with two additional PMOS and NMOS transistor. Over pull up & pull down network of two cascade inverter. In this new circuit NMOS transistor is connected to the pull down network of SRAM cell and other PMOS is connected to the Pull up network of the SRAM cell. The input of the gate of NMOS transistor of pull down network of the SRAM cell is connected V_{dd} and the input gate of PMOS transistor of pull up network of the SRAM cell is connected to ground which keep turn ON the transistor M7 & M8 throughout all operation of the SRAM. This whole modification in the circuit of the SRAM offers better improvement in comparison of 6T. A conventional 6T SRAM consumed more power due to its leakage problem but in the proposed circuit by the adding two transistor at pull up and pull down network leakage is reduced therefore the power consumption of the proposed circuit become less. The proposed improved 8T SRAM cell shows maximum reduction in power consumption of 24.17% with 6T, of 88.6% with 7T, of 28.21% with 8T and of 35.03% with 9T, maximum reduction in delay of 9.1% with 6T, of 64.26% with 7T, of 9.18% with 8T and of 10.44% with 9T and maximum SNM of 35.02% with 6T, of 32.27% with 7T, of 34.4% with 8T and of 33.15% with 9T increases. The read and write operation are similar to conventional 6T.

IV. SIMULATION AND RESULTS

The Simulation and result of the improved 8T SRAM cell is presented in Table 1. In the following subsections, three important metrics of an SRAM design: Static noise margins, power, and delays are explaining.

4.1 STATIC-NOISE-MARGIN (SNM)

The stability of SRAM circuit depends on the Static Noise Margin. The basic SNM is obtained by drawing and mirroring the inverter characteristics and finding the maximum possible square between them. It is a graphical technique of estimating the SNM.

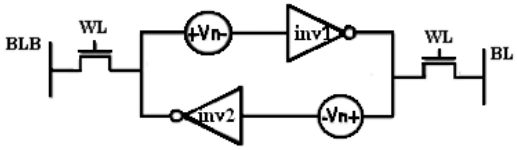

Figure 8 The standard setup for SNM definition

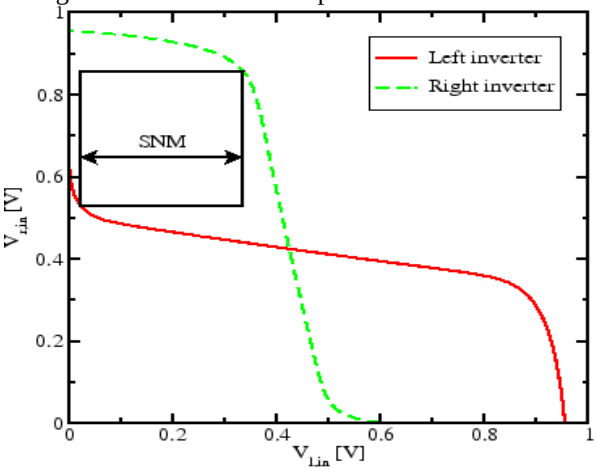

Figure 9 General SNM characteristics during Hold operation

The Figure-9 shows a common way of representing the SNM graphically for a bit-cell holding data. This figure plots the Voltage Transfer Characteristic (VTC) of Inverter 2 (inv2) and the inverse VTC-1 from Inverter 1(inv1). Resulting two-lobed curve is called a 'butterfly curve' and is used to determine the SNM. The length of the side of the largest square that can be embedded inside the lobes of the butterfly curve is defined as the SNM. Consider the case when the value of the noise sources with value Vn are introduced in the bit cell at each of the internal nodes. When the value of Vn increases from 0, it causes the VTC-1 for first inverter in Figure-9 to move downward and the VTC for the

second inverter to move to the right. The values of SNM vary in different operation modes. SNM is becoming important factor to check the stability during read operation. SRAM cell immunity to static noise is measured in terms of SNM that quantifies the maximum amount of voltage noise that can be tolerated at the cross-inverters output nodes without flipping the cell. The value of the SNM during cell operation changes with any change in the noise. Although the SNM is important during hold, the cell stability during active operation represents a more significant limitation to SRAM operation [8].

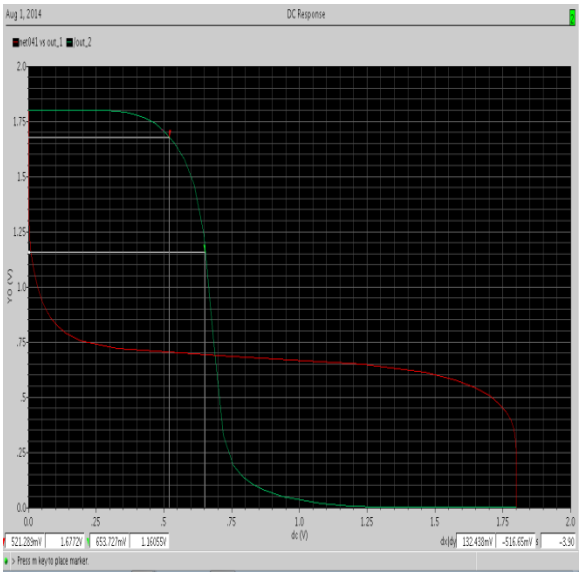

Figure 10 Butterfly curve for SNM of 6T SRAM cell

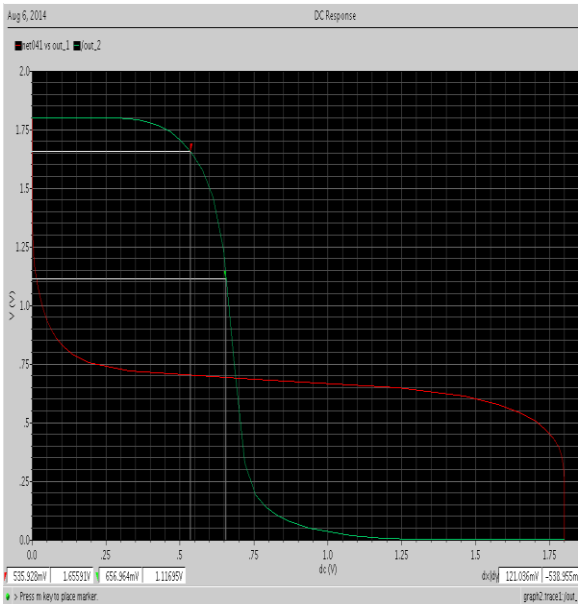

Figure11 Butterfly curve for SNM of 7T SRAM cell

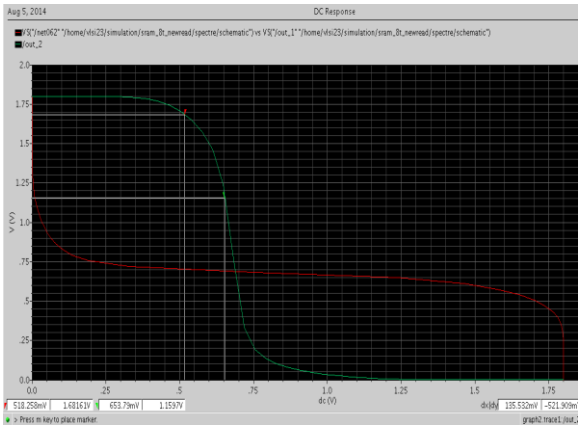

Figure 12 Butterfly curve for SNM of 8T SRAM cell

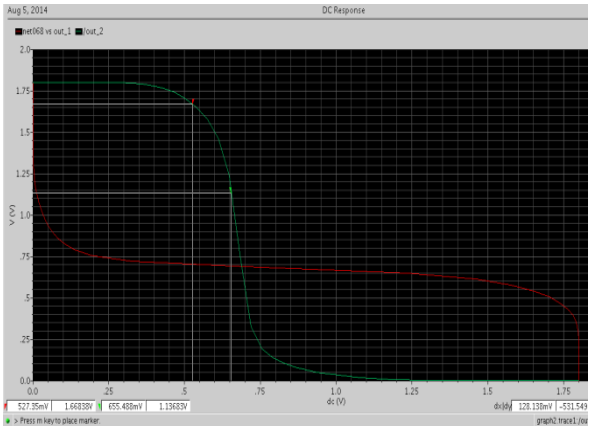

Figure 13 Butterfly curve for SNM of 9T SRAM cell

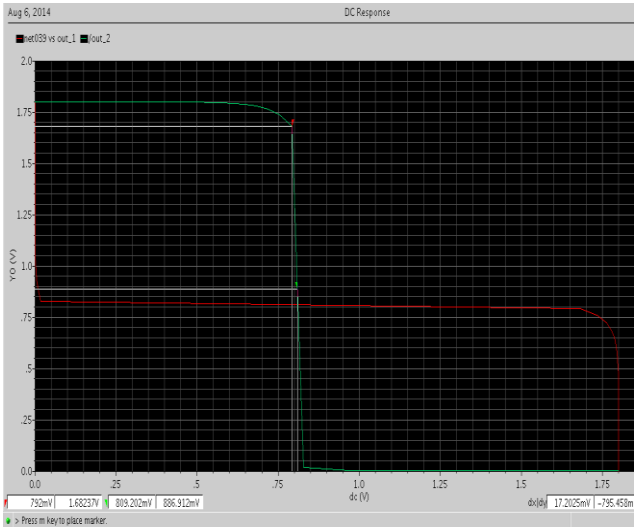

Figure 14 Butterfly curve for SNM of Improved 8T SRAM cell

4.2- DELAY

The delays of SRAM are usually defined as the time it takes to read or write a value from an SRAM cell. While a node is switching, the delay is measured as the time difference between 10% and 90% of the voltage swing. As an example - if we are trying to bring node A from 0V to 1V then the delay is the

time it takes for node A to go from 0.1V to 0.9V. In case of a write operation, write delay is defined as the time required for writing '0'to storage node 'L' from the time when word Line is activated to the time when 'L' falls to 10% of its initial high level. In the same way, writing '1' to 'L' is defined from the time when word Line is activated to the time when 'L' rises to 90% of its full swing from its initial low level. Write delay is approximately equal to the propagation delay of inv2 and inv l [2].

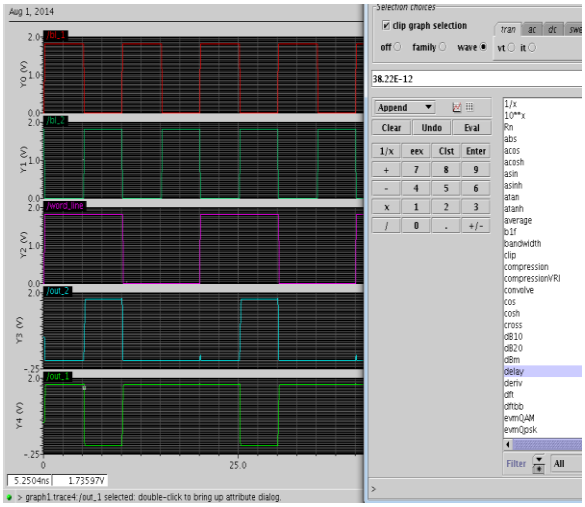

Figure 15 Simulated results for delay of 6T SRAM cell

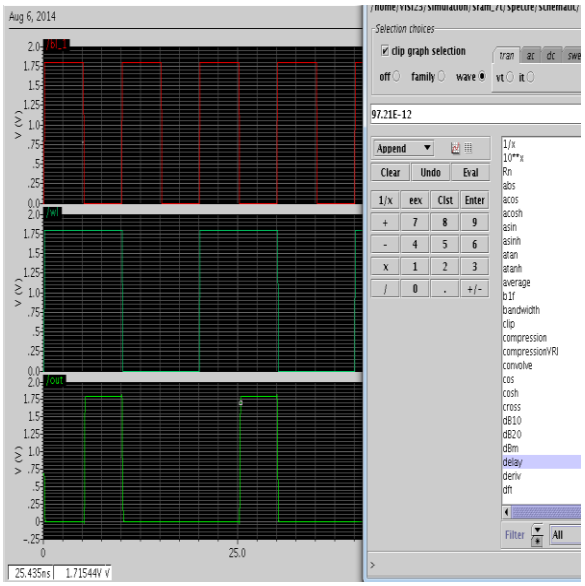

Figure 16 Simulation results for delay of 7T SRAM cell

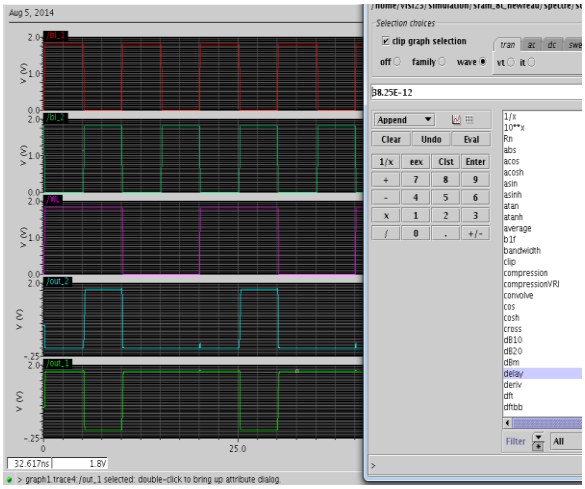

Figure 17 Simulation results for delay of 8T SRAM cell

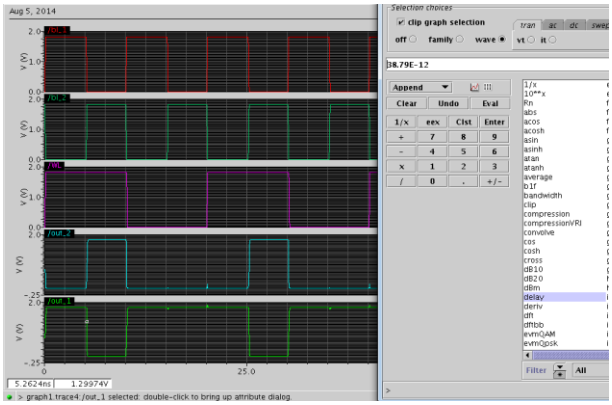

Figure 18 Simulated results for delay of 9T SRAM cell

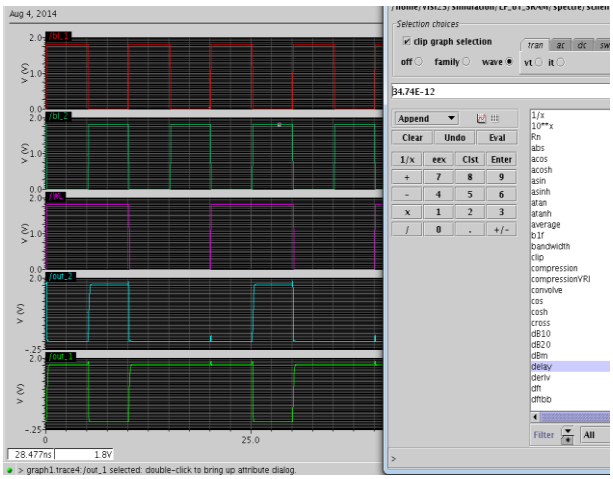

Figure 19 Simulation results for delay of improved 8T SRAM cell

4.3- POWER CONSUMPTION

The power consumption of Static Random Access Memory cell depends on consumption of the power which used to perform the operation of the transistor [5]. Dynamic power consumption in SRAMs is consumed due to the charging and discharging capacitances during read and write operation and during each cycle of SRAM particular amount of Energy is drawn from the power supply and dissipated. For each cycle the power consumption is depended on the type of operation (read or write). Also, when the capacitor charged from GND to VDD and then discharged VDD to GND, the amount of energy drawn from the power supply and dissipated equals $C_L V_{DD}^2$. The stored energy on the capacitor C_L with voltage V_C equals ½ $C_L V_C^2$. Therefore, each time the capacitor C_L is charged from V_C to V_{DD} and then discharged V_{DD} to V_C [3]. A average power dissipation of any device over one period can be obtained by following expression [6].

$$P_{av} = [(1/T) \int_0^T I\, dt] \times V$$

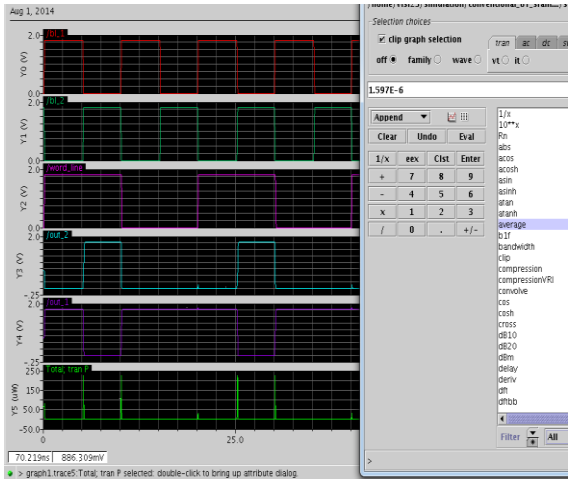

Figure 20 Simulated results for power consumption of 6T SRAM cell

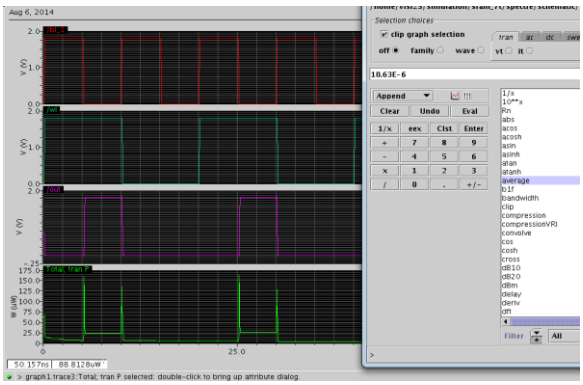

Figure 21 Simulated results for power consumption of 7T SRAM cell

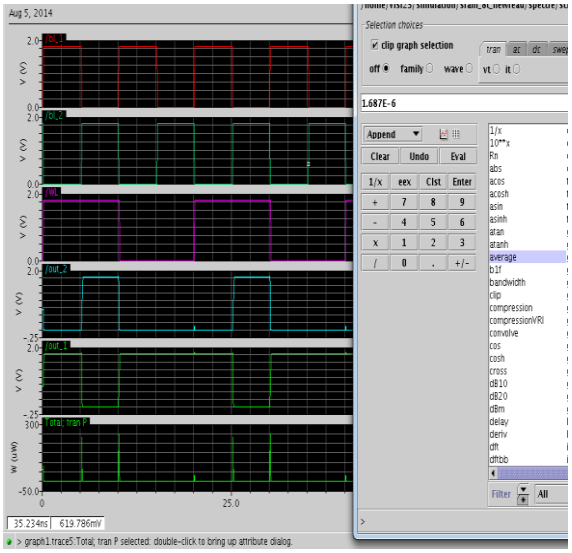

Figure 22 Simulated results for power consumption of 8T SRAM cell

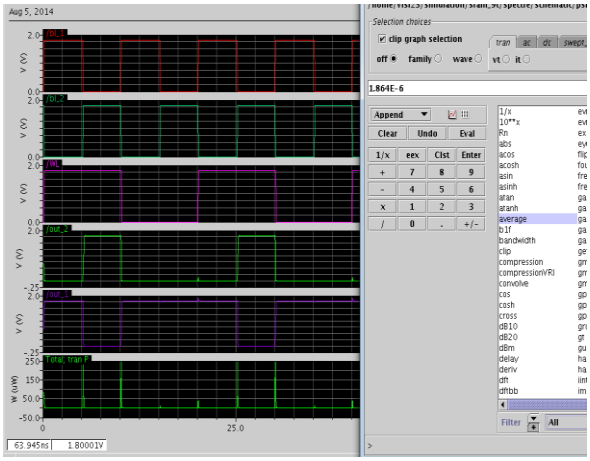

Figure 23 Simulated results for power consumption of 9T SRAM cell

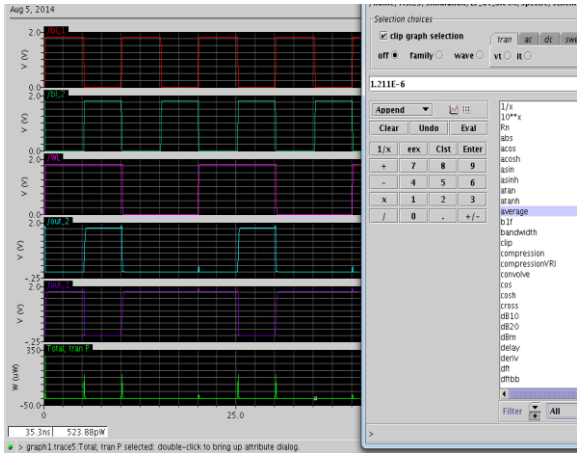

Figure 24 Simulated results for power consumption of improved 8T SRAM cell

Table 1 Comparison of power consumption, delay and SNM.

Parameter	6T	7T	8T	9T	Improved 8T	
Power consumption (µW)	1.597	10.63	1.68	1.86	1.211	
Delay (ps)	38.22	97.21	38.2	38.7	34.74	
SNM (in hold mode)	0.731	0.762	0.738	0.752	1.125	

V. CONCLUSION

In this paper, we have design and implemented a low power, low delay and high SNM SRAM cell. We have also analyzed the power consumption and delay of improved 8T SRAM cell is less as compare to conventional 6T, 7T, 8T, 9T SRAM cell. The improved 8T SRAM cell is reducing the delay and increasing Static Noise Margin (in hold mode). In this paper, The proposed improved 8T SRAM cell shows maximum reduction in power consumption of 24.17% with 6T, of 88.6% with 7T, of 28.21% with 8T and of 35.03% with 9T, maximum reduction in delay of 9.1% with 6T, of 64.26% with 7T, of 9.18% with 8T and of 10.44% with 9T and maximum SNM of 35.02% with 6T, of 32.27% with 7T, of 34.4% with 8T and of 33.15% with 9T increases. Therefore, improved 6T SRAM cell is useful for high-speed and low power applications.

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